Technical and Market Feasibility of High-Speed Software-Reconfigurable OOFDM/DFMA-based Optical Transceivers for Next Generation Access Network PONs

Richard M. Dorward[1], *Fellow IET,* Michael J. Anderson[1], *Member IET,* Roger P. Giddings[2], Member IET
[1] TerOpta Limited, United Kingdom, [2] Bangor University, United Kingdom
Tel: +44 7909 524 719, e-mail: richard.dorward@teropta.com

ABSTRACT
This paper outlines part of the work in the TEROPON project to evaluate the feasibility of developing novel high-speed software-reconfigurable optical transceivers based on Optical Orthogonal Frequency Division Multiplexing (OOFDM) and Digital Filter Multiple Access (DFMA) technologies for Next Generation PONs in the Access Network. It examines the key product requirements, describes some of the experimental work and includes an initial assessment of the technical and market feasibility of these technologies for this application.
Keywords: OOFDM, DFMA, PON, Access Network

1. INTRODUCTION

TEROPON [1] is a short (14-month) project to investigate the technical and market feasibility of developing novel high-speed software-reconfigurable optical transceivers based on Optical Orthogonal Frequency Division Multiplexing (OOFDM) and Digital Filter Multiple Access (DFMA) technologies for SDN-based Next Generation PONs in the Access Network. It builds on the theoretical and experimental results of the earlier FP7 PIANO + OCEAN project, in which both Bangor University and TerOpta Ltd were involved.

The FP7 PIANO+ OCEAN project [1] was a seven party, international, 39 month project, concluding in October 2014, aimed at developing cost effective OOFDM systems for future access networks. Key to the cost effectiveness was delivering capacities of at least 20 Gbit/s over access PONs using commercially available, low cost optical/electrical components, which entailed simple intensity modulation and direct detection (IMDD) schemes. Also considered key to the cost, particularly of the client end ONU, was minimisation of the size of the OOFDM digital processing there, requiring the ONU to process only a fraction of the overall bandwidth in a multiple sub-band architecture, which was implemented initially with analogue filters and mixers. [2]

Unfortunately, GHz analogue filters and mixers do not provide the dynamic software reconfigurability required and involve an additional manufacturing technology, which impacts on the cost, so the final phase of OCEAN introduced the use of reconfigurable digital filter multiplexing. Firstly, a first proof-of-concept real-time experimental demonstration of a two channel point-to-point DFM system [3] successfully multiplexed two independent OFDM signals using orthogonal digital filters, over a 25km SMF, IMDD link. A single FPGA-based transmitter generated and digital-filter-multiplexed two independent multi-Gb/s OFDM signals, the FPGA-based receiver with a single reconfigurable digital filter, successfully demultiplexed and recovered data from either OFDM signal by configuring the digital filter to select the desired channel. This concept was first proposed and investigated by the group at Bangor University and extensive numerical simulations were performed to investigate the digital filtering-induced trade-offs, in terms of upstream transmission capacity, filter design flexibility, and filter DSP complexity in an 8 channel, 8 ONU, DFMA-based PON [4].

This work provides a solid foundation for TEROPON to experimentally evaluate the flexibility of digital filter multiplexing (DFM) techniques and also the benefits of such an OOFDM/DFM combination, particularly in the more demanding upstream direction of a multi-user Next Generation Access PON. The benchmark, against which to measure this, is taken from the ITU-T G.989 Recommendations for Next Generation PONs (NG-PON2) [5], for which the first two recommendations have been published and others in the series are still in progress. The Study Group evaluated a number of technical solutions [6] and a 4-8 channel x 10Gbit/s TWDM architecture was adopted as the lowest risk option, although future research directions included the possibility of new long-term concepts beyond standards if they offered compelling advantages and lower cost.

2. OUTLINE REQUIREMENTS

2.1 Outline Product Requirements

The target TEROPON product requirements are taken directly from the NG-PON2 requirements in the architecture section of G.989.1 but without the specifics of the TWDM architecture.

The minimum requirement is 40 Gbit/s downstream capacity and 10 Gbit/s upstream capacity with a 20 km reach and at least 1:64 split, giving access to peak rates of 10 Gbit/s downstream and 2.5 Gbit/s upstream, with

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flexibility to balance trade-offs in speed, distance, and split ratios for various applications. Other requirements are a passive fibre reach of 40 km, with the ability to reach 60 km, preferably with passive outside plant, access to upstream peak rates also of 10 Gbit/s (shown as crucial by recent market and standards activity [7]) and support for a split ratio of at least 1: 256, with additional flexible logical partitioning to 16k up to 65k ports. The ultimate requirement is to extend the aggregate capacity to 80 Gbit/s.

There is also the requirement for compatibility and co-existence with GPON and XGPON on the same fibre and network plant, which entails operation in the C-and L-bands with specific WDM band filtering, together with a physical layer path loss power budget of a minimum of around 30 dB, and an extended path loss of around 35 dB, both with a post-FEC bit error rate (BER) at the worst case limits of these path losses and other degradations of not worse than 10^{-12}.

Power saving is also an important aspect, especially in the ONUs to maintain the minimum lifeline service(s) as long as possible on loss of mains power, requiring reduced power consumption for low capacity usage.

2.2 Outline Demonstrator Requirements

It is not considered necessary to include all of the physical layer parameters or the software control, as the key project objective is to develop the advanced DSP algorithms for use in future flexible PON transceivers. The project scope requires the use of commercially available hardware e.g. evaluation boards, optical modulators, detectors etc. and a crucial limitation is the maximum operating speed capability of such commercially available hardware and specifically that of the available DAC/ADC combinations of 4 GSamples/s, which, as in OCEAN, allows a transmission rate of around 10 Gbit/s using a 25% OOFDM cyclic prefix and 64QAM.

To match this, the NG-PON2 capacities need to be scaled down by a factor of 4 for the demonstrator, giving capacities of 10 Gbit/s both downstream and upstream, provided as four digitally filtered 2.5 Gbit/s capacity OOFDM sub-bands, allowing access to peak capacities of 2.5 Gbit/s both downstream and upstream. The ONUs should be configurable to provide access to up to 2.5 Gbit/s downstream capacity from any single digitally filtered sub-band, and also to provide a similar upstream capability in any of the digitally filtered sub-bands.

The demonstrator should include operation over 10 – 20 km of fibre and a variety of passive splits at the near and far ends of that fibre, to show the flexibility to balance trade-offs in speed, distance, and split ratios for various applications. The use of different modulation formats should also be included to show the transparency of the DFMA structure to these and the ability to trade-off capacity against ONU power consumption.

The demonstrator should include at least two ONUs and both directions of transmission, to allow evaluation of the benefits of the OOFDM/DFM architecture, particularly in the more demanding upstream direction. To minimise cost, the hardware may be reconfigured to demonstrate the two directions of transmission separately.

3. DEMONSTRATOR

3.1 Demonstrator Architecture

The TEROPON demonstrator architecture is shown in Fig. 1 for the 4 channel upstream case. ONU 1 and ONU 2 can each generate two signals to fill any two of the four DFMA channels by reconfiguring the digital filters appropriately. ONU1 has an Ethernet interface to allow user data to be transported over the PON using either OFDM (high capacity) or PSK (low capacity) modulation. The second signal in ONU 1 and the two signals in ONU 2 are all OFDM modulated PRBS sequences. The OLT contains two reconfigurable digital filters, one is used to select the user data channel and demodulate the signal using either OFDM or PSK, the user data is then directed to an Ethernet interface. The OLT's second filter can select any of the remaining OFDM modulated signals and after demodulation monitors the channel's BER.

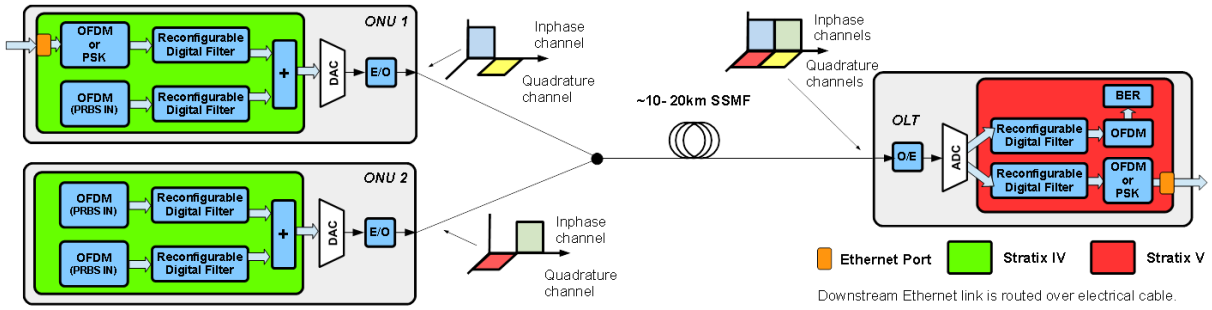

Figure 1. 4 channel DFMA PON Architecture

3.2 Demonstrator Platform

This architecture is implemented in three independent units: one new unit configured as an OLT and two units from the OCEAN project, adapted and configured as ONUs, to demonstrate Multipoint to Point operation.

Each unit consists of an electro-optical interface module, an ADC or DAC, power supply, controller and an FPGA-implemented DSP/Data processor. Configuration and control of each unit is provided through an ARM M3 microcontroller embedded in a MicroSemi Smartfusion, which hosts a web page style interface, accessible over an Ethernet network connection.

Recent advances in FPGA technology have made available increased resources on a single chip, e.g. multiplier cells, which are advantageous for DSP functions such as FFTs and digital filters, plus advanced high speed (~1 Gbs) I/O with Serialiser/Deserialiser functions to create high bandwidth parallel busses. In this project, the ONUs used Altera Stratix IV devices and the OLT an Altera Stratix V GS, which offers 3180 multipliers.

The ADCs were from E2V and, in common with any ADC using an interleaved architecture, required a calibration activity, entailing frequency domain analysis of each ADC channel [8], to achieve the best possible performance. Silicon process variations lead to differences in parameters such as offset, gain and phase of the interleaved ADC's, which introduces a source of noise in the system unless corrected. In this instance the parameters were normalised to $\pm$ 0.16 LSB offset, $\pm$ 0.06% gain and $\pm$ 100 fs phase .

Figure 2. Demonstrator OLT and one ONU

This calibration process and the commercial availability and adaptation of a compatible ADC and FPGA combination for the OLT occupied a large part of the experimental effort, delaying the main experimental work.

3.3 Experimental Results

Using a bench-top real-time 2 channel DFMA transmitter(s) and a high-speed digital storage oscilloscope (DSO) running MatLab as an off-line receiver, some key experimental results have been achieved. Firstly, to combat channel response-induced cross-channel interference between two orthogonal DFMA channels a cross-channel interference cancelation (CCIC) technique [9] has been developed and experimentally demonstrated. The technique detects both orthogonal channels and based on knowledge of the system channel response, the DFMA filter responses and the received signal on one channel, an estimate of the interference on the other channel is obtained. The estimated interference is then subtracted from the received signal on the other orthogonal channel. Using OFDM signals on each channel, the results have shown that for a channel response roll-off of ~11dB, with only a single iteration the CCIC technique can achieve; i) improvements in individual subcarrier BERs of over 1000 times, ii) improvements in channel capacity of up to 19 times and iii) power budget improvements of up to 3.5dB. Secondly, a 2 channel DFMA-PON has been successfully demonstrated over 25km SSMF. Two real-time OFDM-DFMA transmitters each generated an orthogonal channel, the two channels were then combined in the optical coupler in the PON. The offline receiver successfully recovered the OFDM-modulated data from either channel by selecting the appropriate filter coefficients. This is a key milestone as it is the first proof-of-concept experiment of multipoint-to-point transmission using the DFMA-PON technique.

Results using the full, real-time demonstrator equipment are awaited at the time of submission of this paper.

4. EXTRAPOLATION TO FULL NG-PON CAPABILITY AND ASIC IMPLEMENTATION

4.1 Logical Extrapolation

The key requirements, in terms of the digital processing in particular, are a downstream capacity of 40 Gbit/s, a physical split ratio of at least 1: 256 and access to peak rates of 10 Gbit/s both downstream and upstream at an ONU. The peak rate access means that there must be a much finer granularity than $1/256^{th}$ of the aggregate capacity to allow one or more ONUs to access rates of 10 Gbit/s, while still preserving lower rates for the remaining ONUs (hence the need for additional logical partitioning).

The basic unit of partitioning in an OOFDM/DFMA architecture is a single subcarrier, and the OOFDM N-point FFT multiplier count scales up as $(N/2)\ \log_2 N$ for N/2 subcarriers. Also, the complexity due to the filtering does not scale linearly with channel count: due to the up-sampling significant numbers of transmit filter taps are redundant (zero valued coefficients) and due to the down-sampling and parallel filter structure complete filters are redundant in the receiver. However, partitioning of the total number of subcarriers into a number of channels reduces the size of each FFT, so there can be a trade-off, particularly in the case of the ONU.

Three cases of the total number of subcarriers were considered. A conceptual lower bound was taken as 511 subcarriers, allowing two ONUs to each access rates of 10 Gbit/s, while still leaving 20 Gbit/s for the remaining maximum of 254 ONUs, but with no flexibility left for these. Then the other cases were the NG-PON2 specified additional logical partitioning of 16k and 64k. In each case the number of channels was varied between the

minimum 4 in the demonstrator and a maximum of 256, corresponding to the specified physical split. Other key parameters were using 16-QAM, rather than 64-QAM, due to multi-channel interference and hence a 24 GSamples/s ADC/DAC rate to maintain an aggregate 40 Gbit/s, and an ASIC/FPGA maximum clock rate of 500 MHz.

The resulting ONU size/complexity was taken as the number of complex multipliers used, as this was assessed to be by far the dominant factor. Figure 3 shows the result of these calculations: an enormous reduction in complexity with increasing DFMA channel count, compared with the simple OOFDMA case, and only a factor of ~4 between the optimum values across this very wide range of total subcarriers.

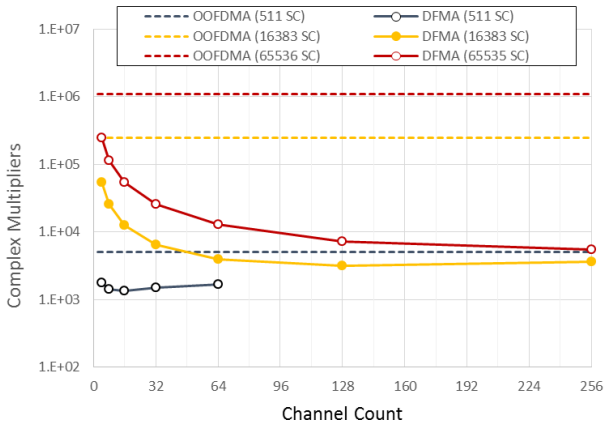

Figure 3. Complexity vs. Channel and Subcarrier counts

4.2 ASIC Implementation

The optimum numbers of multipliers are easily within the range of the new Stratix 10 FPGA (with 14 nm technology core) and so must be readily realisable in custom ASIC form. However, the ADC and DAC are much more critical and need to be integrated with the logic for cost and power consumption reasons. Currently, only Fujitsu offer such monolithic integration on a commercial basis, with an interleaved 56 GSamples/s ADC/DAC capability. However, other PON system vendors have internal proprietary capabilities, which could potentially be considered if they were interested in adopting this OOFDM/DFMA technology.

5. SUMMARY AND CONCLUSIONS

The current ITU-T Recommendations have been analysed to extract the key outline product requirements that any technology has to meet to be a candidate contender for Next Generation Access PON systems.

Starting from the OOFDM work under OCEAN, the TEROPON project has demonstrated, on paper at least so far, that the addition of the DFMA technique has the capability to massively reduce the logical complexity of a simple OOFDMA solution to the point where even the most extended logical partitioning flexibility, demanded in the ITU-T Recommendations, should be readily realisable within current ASIC technology. The optimum number of DFMA channels needs to be further studied, but the basic technical feasibility has been established.

The real-time experimental work needs to be completed to evaluate how well the digital filtering technique can be made to work in practice and to identify whether there are any further unexpected issues to address. However, a major finding so far is the technology, and potentially time and cost, issues associated with the use of interleaved ADCs. These will have to be addressed within the control of the ASIC processing in any future commercial implementation using this OOFDM/DFMA technique.

Also outstanding is evaluating with any PON system vendor how the system capabilities and ASIC complexity compare with the already standardised TWDM PON technology, to establish the real market feasibility of the OOFDM/DFMA technique for this application. Discussions are currently starting with one vendor.

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